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Jones Art Unit 212

S. N. 667,691 11/02/84

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Before the Board of Appeals

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FOR

APPELLANT

Examiner's Answer

1. Examiner's Answer

2. (1) Status of claims .

3. The statement of the status of claims contained in the brief is incorrect.

A correct statement of the status of the claims is as follows:

Appellant provided no statement of the status of the claims. Claims 1-26 are rejected under the judicially created doctrine of obvious-type double patenting. Claims 7-10, 17 and 18 are additionally rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tanaka et al. Claim 11 is also rejected under 35 U.S.C. 103 as being obvious in view of Tanaka et al. Claims 12-16 are additionally rejected under 35 U.S.C. 103 as being obvious in view of Zansky and Sullivan.

4. This appeal involves claims 1-26.

5. (2) Status of Amendments After Final .

6. No amendment after final has been filed.

7. (3) Summary of invention .

Appellant provided no statement of summary of the invention. Claim 1 however, summarize the invention as follows:

1. A power supply adapted to be powered from a source of relatively low frequency periodic DC voltage

pulses and operable to provide a relatively high frequency AC output voltage to a load, said DC voltage pulses having a pulse period and being characterized by exhibiting a relatively high magnitude during part of said pulse period and a relatively low magnitude during the remainder of said pulse period, said power supply comprising:

inverter means connected with said source and conditionally operative to convert said low frequency periodic DC voltage pulses into said high frequency AC output voltage, said inverter means having a pair of control terminals adapted to receive a control voltage operable to selectively place said inverter means into either of two states:

State A wherein said inverter means is operative to convert said DC voltage pulses into said high frequency AC output voltage, thereby to provide said high frequency AC output voltage to said load; or

State B wherein said inverter means is operative not to convert said DC voltage pulses into said high frequency AC output voltage, thereby not to provide said high frequency AC output voltage to said load.

8. (4) Issues .

The issues on Appeal are whether claims 1-26 are properly rejected under 35 U.S.C. 112, whether claims 7-9, 17 and 18 are properly rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tanaka et

al. and whether claims 12-16 are properly rejected under 35 U.S.C. 103 as being obvious in view of Zansky and Sullivan.

9. (5) Grouping of Claims .

10. The rejection of claims 1-26 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together. See 37 CFR 1.192(c)(5).

11. (6) Claims appealed .

The copy of the appealed claims contained in the Appendix to the brief is correct.

12. (7) Prior Art of record .

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,506,318	Nilssen	3-1985
4,467,246	Tanaka et al.	9-1984
4,317,165	Sullivan	2-1982
4,523,131	Zansky	6-1985

13. (8) New prior art .

No new prior art has been applied in this examiner's answer.

14. (9) Grounds of rejection .

The following ground(s) of rejection are applicable to the appealed claims.

Claims 1-26 are rejected under the judicially created doctrine of obviousness type double patenting because Appellant's broad recitation of "control terminals" in claim 1 of the instant application is obvious over the control terminals of potentiometer 83 as shown in figure 1 of Appellant's prior patent 4,506,318. Claims 7-10, 17 and 18 are rejected under U.S.C. 102(b) as being anticipated by Tanaka et al. In regard to claims 7, 8 and 9, the word "conditionally" as used in the phrases "conditionally operative" and "conditionally self-oscillating" does not provide a patentable restriction as all circuits including all oscillators operate under some conditions and fail to operate under other conditions. Tanaka et al. discloses an inverter which converts a dc input into an ac output, a self-oscillating circuit and electrically responsive control means consisting of transistor TR3 as described in column 3 lines 51 to 55. In regard to claims 17 and 18, Tanaka discloses the self oscillating inverter, the source of DC voltage and the AC output with the trigger means being viewed as being the on signal for transistor TR3 and the disabling means the off signal for TR3. The on period of TR3 is substantially longer than the period of the AC voltage output. Claims 12-16 are rejected under U.S.C. 103 as being obvious in view of Zansky and Sullivan. Zansky discloses the frequency converter which converts 60Hz line frequency voltage into high frequency output voltage with electrically actuable control means 149 operable to control the RMS magnitude

of the output voltage, said control means going to operational amplifier A3 as discussed in column 8 lines 27 to 32. Zansky further discloses measuring lamp current in column 7 lines 53 to 56 but does not disclose measuring RMS magnitude output voltage. However, Sullivan et al. discloses measuring RMS voltages in the last sentence of his abstract. Sullivan further discloses using the detected RMS values for pulse width control in the same sentence. Zansky has similarly disclosed using his measured lamp current value for pulse width control in column 2 lines 59 to 61. Given that they are both inverters using pulse width modulation to control inverter output, it would have been obvious to one skilled in the art to have adapted the RMS measurement and control of Sullivan in the pulse width control means of Zansky in order to achieve a more accurate means of measurement and control. In regard to claim 13, light loads which do not distort the output of a power supply are known in the art. Connection of a power supply to such a load is viewed to be an obvious design choice and therefore is given no patentable weight. In regard to claim 14, Zansky discloses an output which a "chopped pulse train of a value which is instantaneously proportional to the main supply voltage". This is viewed to be a substantially square wave voltage. In regard to claim 15, light loads which do not distort the output of a power supply are known in the art. Connection of a power supply to such a load is viewed to have been a design choice which would have

been obvious to one skilled in the art. In regard to claim 16, Zansky recites in column 3 line 63 to 66 that "The power supply... provides a chopped current pulse train of a value which is instantaneously linearly proportional to the main supply voltage". Zansky further states in column 8 lines 12 to 15, "the system forces the current and voltage forms to be in phase at all times".

15. (10) New ground of rejection .

This examiner's answer contains the following NEW GROUND OF REJECTION.

Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. and claim 11 is rejected under 35 U.S.C. 103 as being obvious in view of Tanaka et al. In regard to claim 10, the transistor TR3 turns the output voltage on and off and therefore inherently controls the RMS magnitude of the AC output voltage by changing it from some positive value to zero. In regard to claim 11, the circuit of Tanaka is designed to be connected to a load and therefore fulfilling the intended purpose of the device by connecting it to a load is given no patentable weight. In regard to the RMS magnitude being independent of the nature of the load, light loads are known in the art and connection of the power supply to such a light load would result in satisfying the limitations of this claim. The phrase "nature of the load" is viewed as referring to resistive, inductive or capacitive loads.

16. (11) Response to argument .

In regard to the obvious-type double patenting rejection, the limitation which has been added to claim 1 by this C.I.P. is the recitation of "a pair of control terminals adapted to receive a control voltage operable to selectively place said inverter means into either of two states". Applicant's patent number 4,506,318 discloses phase point triggering in column 5, lines 64-68 as controlled by R2, R3, and C3. Furthermore applicant point out in column 6, lines 34-40 of said patent, that the magnitude of R2 and R3 can be set to prevent triggering of the inverter during the entire duration of a given DC pulse. State "B" of claim 1 is this same nontriggering state as set forth above in regard to the 4,506,318 circuit operation. Potentiometer R3 selectively controls such a state. The control terminals of potentiometer R3 selectively place the inverter in states A and B of claim 1 and thus satisfy the claim language.

17. In regard to Appellant's arguments concerning claims 7-9, 17 and 18, Appellant states in his argument, "Tanaka's inverter means is unconditionally self-oscillating if connected with its DC supply voltage". Being connected to the supply voltage is a conditional limitation on the functioning of the inverter which meets Appellant's claim language of "conditionally operable". In this instance and also in regard to the trigger means recited in claims 17 and 18 Appellant tries to read precise limitations into broad claim

language. A trigger means is nothing more than a means of turning a device on or off. If Appellant intends his claim to more narrowly define the invention, he has to use more precise claim language.

18. Regard to Appellant's arguments concerning claim 11, it is not clear what Appellant fails to understand in regard to the rejection. Once again it would appear that Appellant is reading into his broad claim language limitations which do not exist. The claim recites "a load" and therefore any kind of load meets the claim language. While claim 11 does not specifically define "light loads", a light load does satisfy the claim language.

19. In regard to the rejection of claim 12, Examiner was referring to element 149, not resistor 49. Element 149 is a DC voltage set point input. As Zansky recites in column 8 lines 24 to 44, the average lamp current is proportional to the average DC voltage. Thus if you control one you inherently control the other.

20. In regard to Appellant's arguments concerning the combination of references and the hypothetical person skilled in the art, these arguments were raised and laid to rest in In re Nilssen, 7 USPQ 2d 1500 (CCPA 1988). In regard to Appellant's arguments concerning the legitimacy of the judicially created doctrine of obviousness-type double patenting, the most relevant case law is In re Vogel 164 USPQ 619. While Appellant may not like or agree with the doctrine of obviousness-type double patenting, the doctrine is well-established

in patent law. For the above reasons, it is believed that the rejections should be sustained.

(12) Period of response to new ground of rejection.

In view of the new ground of rejection, appellant is given a period of TWO (2) MONTHS from the mailing date of this examiner's answer within which to file a reply to any new ground of rejection. Such reply may include any amendment or material appropriate to the new ground of rejection. Prosecution otherwise remains closed. Failure to respond to the new ground of rejection will result in dismissals of the appeal of the claims so rejected.

Respectively submitted,

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ART UNIT 212